WHAT IS CLAIMED IS:

1. A method of fabricating a semiconductor device comprising a wafer treatment step performing prescribed treatment on a first part having a prescribed etching property and a second part having an etching property different from said prescribed etching property, formed on a semiconductor substrate, in a chamber with gas for etching, wherein

said wafer treatment step includes an etching gas supply step of introducing said gas for etching into said chamber, and

assuming that a time between introduction of said gas for etching into said chamber and starting of etching of said first part is referred to as a first starting time and a time between introduction of said gas for etching into said chamber and starting of etching of said second part is referred to as a second starting time longer than said first starting time,

a time for carrying out said etching gas supply step is longer than said first starting time and shorter than said second starting time.

2. The method of fabricating a semiconductor device according to claim 1, wherein

the time difference between said first starting time and said second starting time is not more than about 5 seconds.

3. The method of fabricating a semiconductor device according to claim 1, further comprising steps of:

forming an insulator film on said semiconductor substrate, and

forming a conductive region on said insulator film, wherein

said step of forming said insulator film includes a step of forming a gate insulator film,

said step of forming said conductive region includes a step of forming a gate electrode part on said gate insulator film,

said first part contains a reaction product generated before forming said gate electrode part for covering the surface of said gate insulator film and the surface of said gate electrode part,

said second part includes said gate insulator film, and

said gas for etching includes hydrofluoric acid gas.

4. The method of fabricating a semiconductor device according to claim 1, wherein

said wafer treatment step includes an added gas supply step of introducing reaction accelerating gas for further reducing said first starting time into said chamber before said etching gas supply step.

5. The method of fabricating a semiconductor device according to claim 4, wherein

said added gas supply step and said etching gas supply step are alternately carried out in said wafer treatment step.

6. The method of fabricating a semiconductor device according to claim 4, wherein

said added gas supply step is continuously carried out also after said etching gas supply step is started in said wafer treatment step.

7. The method of fabricating a semiconductor device according to claim 1, wherein

said wafer treatment step includes an evacuation step of evacuating said chamber, and

said evacuation step is not carried out at least while said etching gas supply step is carried out.

8. The method of fabricating a semiconductor device according to claim 1, further comprising steps of:

forming a conductive layer on said semiconductor substrate through a gate insulator film,

forming a layer for defining a mask on said conductive layer,

etching said conductive layer through a mask of said layer for defining a mask thereby forming a gate electrode, and

removing said layer for defining a mask remaining on said gate electrode after formation of said gate electrode, wherein

said wafer treatment step includes a step of removing said layer for defining a mask,

said first part includes said layer for defining a mask,

said second part includes said gate insulator film, and

hydrofluoric acid gas is supplied as etching gas in said etching gas supply step.

9. The method of fabricating a semiconductor device according to claim 8, wherein

said etching gas supply step is repetitively carried out in said wafer treatment step.

10. The method of fabricating a semiconductor device according to claim 9, wherein

said wafer treatment step includes an evacuation step evacuating said chamber, and

said etching gas supply step and said evacuation step are alternately carried out.

11. A wafer treatment apparatus for performing prescribed treatment on a first part having a prescribed etching property and a second part having an etching property different from said prescribed etching property, formed on a wafer, with gas for etching, comprising:

a chamber storing said wafer;

an etching gas supply part supplying said gas for etching into said chamber; and

a control part controlling supply of said gas for etching from said etching gas supply part into said chamber, wherein

said control part has, assuming that a time between introduction of said gas for etching into said chamber and starting of etching of said first part is referred to as a first starting time and a time between introduction

of said gas for etching into said chamber and starting of etching of said second part is referred to as a second starting time longer than said first starting time, a function of supplying said gas for etching from said etching gas supply part into said chamber by a time longer than said first starting time and shorter than said second starting time.

12. The wafer treatment apparatus according to claim 11, wherein the time difference between said first starting time and said second starting time is not more than about 5 seconds.

13. The wafer treatment apparatus according to claim 11, further comprising:

an added gas supply part supplying reaction accelerating gas for reducing said first starting time into said chamber, wherein

said control part includes a function of supplying said reaction accelerating gas from said added gas supply part into said chamber before supplying said gas for etching.

14. The wafer treatment apparatus according to claim 13, wherein said control part includes a function of alternately supplying said gas for etching and said reaction accelerating gas.

15. The wafer treatment apparatus according to claim 13, wherein said control part includes a function of supplying said reaction accelerating gas also while supplying said gas for etching.

16. The wafer treatment apparatus according to claim 11, further comprising:

an evacuation part evacuating said chamber, wherein

said control part includes a function of not operating said evacuation part at least while supplying said etching gas.

17. A cleaning method after formation of a gate electrode, removing

a reaction product formed by etching with hydrofluoric acid gas after forming a gate electrode patterned by said etching with a mask on a semiconductor substrate through a gate insulating film.

18. The cleaning method after formation of a gate electrode according to claim 17, wherein

the time for removing said reaction product with said hydrofluoric acid gas is within the reaction time difference between a time when said reaction product is scraped by said hydrofluoric acid gas and a time when said gate insulator film is scraped.

19. The cleaning method after formation of a gate electrode according to claim 18, wherein

said reaction time difference is repetitively set thereby removing said reaction product with said hydrofluoric acid gas.

20. The cleaning method after formation of a gate electrode according to claim 19, wherein

said semiconductor substrate formed with said gate electrode is set in a chamber, and said reaction time difference is repetitively set by repeating steps of evacuating said chamber and charging said chamber with said hydrofluoric acid gas.